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ARCHITECTURE THAT CONVERTS A HALF-DUPLEX BUS TO A FULL-DUPLEX BUS WHILE KEEPING THE BANDWIDTH OF THE BUS CONSTANT

Field of the Invention

The present invention relates to a method and/or architecture for converting a half-duplex bus to a full-duplex bus generally and, more particularly, to converting a half-duplex bus to a full-duplex bus while maintaining a constant bandwidth.

Background of the Invention

Referring to FIG. 1, a block diagram of a circuit 10 illustrating a half-duplex bus architecture is shown. The circuit 10 includes a bi-directional bus with a plurality of half-duplex channels that only support half-duplex communication. The circuit 10 can connect a first circuit (card) 12 to a second circuit (card) 14. The circuits 12 and 14 can exchange data via transmission lines (pairs of wires) 16. Each pair of wires 16 can be used to transmit or receive data at a rate of 77.75MB/s. At each end of each pair of wires 16, an output buffer 18 and an input buffer 20 are connected together. Connecting the input buffer 20 and output buffer 18 together can result in a bus contention when the output

buffers (transmitters) 18 at both ends of the transmission lines 16 are active. Depending on buffer (driver) type, additional circuits can be required to prevent the output buffers 18 from self-destructing. The addition of the input buffer 20 in parallel with the output buffer 18 can increase capacitance of the source and destination end of the transmission lines 16. The increased capacitance can affect the termination-impedance of the transmission lines 16.

The conventional half-duplex bus can have the following disadvantages: 1. bus contention during hot insertion of cards (e.g., both output buffers 18 of a channel 16 can be ON at the same time); 2. half-duplex operation (i.e., only one card can transmit at one time); 3. additional components can be required to prevent the destruction of the output buffers 18; 4. termination at both ends of the transmission line places increased load and current-drive requirements on the enabled output buffer 18; 5. bus turn-around can require phase lock loops (PLLs) to re-acquire lock, therefore, slowing data exchange.

A conventional method for providing a full-duplex bidirectional bus is to use a hybrid network to allow simultaneous bi-directional transmission of data across the same pair of wires.

The drawback to a hybrid circuit is that the hybrid networks can require echo cancellation circuits which can require a 6dB or better signal to noise ratio (SNR). The hybrid circuit can also require receivers with greater sensitivity or larger source amplitude for valid transmission. The greater sensitivity and large source amplitude can result in greater power dissipation, higher complexity, and possibly greater radiated emissions.

Summary of the Invention

The present invention concerns an architecture comprising a first circuit, a second circuit, and one or more pairs of communication channels. The first circuit may be configured to transmit one or more first serial streams in response to a plurality of first source data streams and recover a plurality of second source data streams from one or more second serial streams. The second circuit may be configured to transmit the one or more second serial streams in response to the plurality of second source data streams and recover the plurality of first source data streams in response to the one or more first serial streams. The first circuit and the second circuit may be coupled by the one or more

pairs of communication channels. The first and second circuits may be configured to transmit simultaneously.

The objects, features and advantages of the present invention include providing an architecture that converts a half-duplex bus into a full-duplex bus that may (i) convert a bus architecture comprising a plurality of half-duplex channels into a full-duplex bus comprising a plurality of simplex channels; (ii) double the throughput of the bus while maintaining a constant bus bandwidth; and/or (iii) reduce the number of physical channels by interleaving three or more data character streams and multiplying the channel speed.

Brief Description of the Drawings

These and other objects, features and advantages of the present invention will be apparent from the following detailed description and the appended claims and drawings in which:

FIG. 1 is a block diagram of a half-duplex bus design;

FIG. 2 is a block diagram of a preferred embodiment of the present invention;

FIG. 3 is a detailed block diagram of the circuit of FIG. 2;

FIG. 4 is a more detailed block diagram of the circuit of FIG. 3;

FIG. 5 is a block diagram illustrating an example operation of the present invention; and

FIG. 6 is a block diagram of an alternative embodiment of the present invention.

Detailed Description of the Preferred Embodiments

Referring to FIG. 2, a block diagram of a circuit 100 is shown illustrating a preferred embodiment of the present invention. The circuit 100 may be implemented as a full-duplex bus comprising a plurality of simplex channels. In one example, the circuit 100 may be implemented as part of a backplane or motherboard of a computer, controller, or other device. Alternatively, the circuit 100 may be implemented as part of a network. The circuit 100 may be configured to communicate a number of source data streams (e.g., A_SRC1-A_SRCN, where N is an integer) from a circuit (host) 102 to a circuit (host) 104 and a number of source data streams (e.g., B_SRC1-B_SRCN, where N is an integer) from the circuit 104 to the circuit 102. The circuits 102 and 104 may be implemented, in one example, as peripheral devices (e.g., cards). In one example, the

source data streams may have a data rate of 77.75 MB/s. However, other data rates may be implemented accordingly to meet the design criteria of a particular application. The source data streams may be implemented as character (parallel data) streams.

The circuit 100 may comprise a circuit 112, a circuit 114, a number of transmitters 116 and a number of receivers 118. The circuits 112 and 114 may be implemented as interleaving/de-interleaving (multiplexing/de-multiplexing) circuits. The circuits 112 and 114 may be configured to (i) generate one or more serial streams (e.g., A_SER1-A_SERM or B_SER1-B_SERM, where M is an integer) by interleaving, encoding, and/or serializing the number of source data streams A_SRC1-A_SRCN or B_SRC1-B_SRCN and (ii) recover the source data streams A_SRC1-A_SRCN and B_SRC1-B_SRCN by de-interleaving, decoding, and/or de-serializing the one or more serial streams A_SER1-A_SERM and B_SER1-B_SERM, respectively. The value M may be less than or equal to the value N. For example, M may equal N when no interleaving is desired. The serial streams generally have a data rate that is a multiple of the data rate of the source data streams. The multiplier is generally a product of the interleave ratio and a parallel-to-serial conversion ratio. In one example, the serial streams may have a signaling rate of

1555 MBd when the source data streams have a data rate of 77.75 MB/s, the interleave ratio is 2:1, and the parallel-to-serial conversion ratio is 10.

Each of the transmitters 116 may be connected to a receiver 118 by a simplex serial channel 120. The simplex serial channel 120 may be implemented, in one example, as a pair of wires. Alternatively, the simplex serial channel 120 may be implemented using fiberoptic, coaxial, twisted pair, microstrip, stripline, or other appropriate transmission line technology. In one example, a full-duplex bus 122 may be implemented by pairing two of the simplex serial channels 120.

The circuit 102 may have a number of outputs 104a-104n that may present the source data streams A_SRC1-A_SRCN and a number of inputs 106a-106n that may receive the source data streams B_SRC1-B_SRCN. The circuit 104 may have a number of outputs 108a-108n that may present the source data streams B_SRC1-B_SRCN and a number of inputs 110a-110n that may receive the source data streams A_SRC1-A_SRCN.

The circuit 112 may have a number of outputs that may present each of the signals A_SER1-A_SERM to an input of a transmitter 116. The transmitters 116 may transmit the signals

A_SER1-A_SERM to respective receivers 118. The receivers 118 may present the signals A_SER1-A_SERM to a respective input of the circuit 114. The circuit 114 may have a number of outputs that may present each of the signals B_SER1-B_SERM to an input of a respective transmitter 116. The transmitters 116 may communicate the signals B_SER1-B_SERM to respective receivers 118. The receivers 118 may present the signals B_SER1-B_SERM to inputs of the circuit 112.

The circuits 112 and 114 may be configured to interleave a number of source data (character) streams to generate one or more serial streams and de-interleave the one or more serial streams to recover the number of source data (character) streams. In one example, the circuits 112 and 114 may be configured to receive a plurality of serial streams. The serial streams may be skewed by delay variations between the serial channels (links) 120. The circuits 112 and 114 may be configured to (i) deserialize and decode the received serial streams back into interleaved data (character) streams and (ii) bond the interleaved data (character) streams to align the data (characters) before de-interleaving.

As used herein, bonding generally refers to an operation bringing two (or more) streams of data, where all streams operate

at the exact same character (or serial) rate but are received in arbitrary phase relative to each other, into a common phase alignment. Bonding (or operating with bonded channels) allows multiple links to operate as a single link. A bonding operation generally begins by detecting a specific event or events at the receive end of the links that was generated at the transmit end of each link when the streams were in the desired alignment. The event detected may be, for example, a specific character or sequence of characters (e.g., for links using character based framing) or a distributed marker that may be found repetitively at predetermined locations within each data stream. When the specific event or events is detected, the streams at the receive end may be re-aligned to the desired alignment. An example of channel bonding may be found in the co-pending application, U.S. Ser. No. 09/822,979, which is hereby incorporated by reference in its entirety.

Each end of the full-duplex bus formed by the serial links 120 may have, in one example, two transmitters 116 and two receivers 118. However, other numbers of transmitters and receivers may be implemented to meet the design criteria of a particular application. Both transmitters 116 may be transmitting

all of the time at a signaling rate that is, in one example, twenty times the data rate of the source data (character) streams (e.g., the signaling rate of the transmitters 116 may be 1555 MBd when the source data rate is 77.75 MB/s, the interleave ratio is 2:1 and the parallel-to-serial conversion ratio is 10). To maintain the four distinct channels found in the architecture shown in FIG. 1, the circuits 112 and 114 may be configured to interleave two source character streams (e.g., A_SRC1 with A_SRC2, A_SRC3 with A_SRCN, B_SRC1 with B_SRC2, and B_SRC3 with B_SRCN) into a single interleaved data stream for transmission as a serial stream (e.g., A_SER1, A_SERM, B_SER1, and B_SERM, respectively) with a signaling rate that is, in one example, twenty times that of the parallel interface character-rate clock. At the receive end of the serial channels 120, the serial streams may be converted back to interleaved data streams that may be aligned to a common time reference by the bonding process. When the interleaved data streams are bonded, the characters in each channel may be de-interleaved back into the respective source data (character) streams (e.g., A_SRC1-A_SRCN and B_SRC1-B_SRCN).

Referring to FIG. 3, a block diagram of the circuit 112 of FIG. 2 is shown. The circuit 112 and the circuit 114 may be

implemented similarly. As such, only the circuit 112 is described for brevity. The circuit 112 may comprise a circuit 140 and a circuit 142. The circuit 140 may be configured to generate the serial streams A_SER1-A_SERM in response to the source data streams A_SRC1-A_SRCM. The number of source data streams N may be larger than or equal to the number of serial streams M. In one example, N may be an integer multiple of M. The circuit 142 may be configured to recover a number of source data streams from one or more serial streams. For example, the circuit 142 may recover the source data streams B_SRC1-B_SCRN from the serial streams B_SER1-B_SERM.

The circuit 140 may comprise a circuit 144 and a circuit 146. The circuit 144 may be implemented as an interleaver circuit. The circuit 146 may be implemented as an encoder and serializer circuit. The signals A_SRC1-A_SRCN may be presented to a number of inputs 148a-148n of the circuit 144. The circuit 144 may have a number of outputs 150a-150m that may present a number of interleaved data (character) streams (e.g., A_INT1-A_INTM) to a number of inputs 152a-152m of the circuit 146. Each of the signals A_INT1-A_INTM may be generated by interleaving (multiplexing) data from two or more source data streams. In one example, two source

data streams may be interleaved to form one interleaved data stream. The circuit 146 may have a number of outputs 154a-154m that may present the signals (serial data streams) A_SER1-A_SERM. The signals A_SER1-A_SERM may be generated by encoding and serializing the signals A_INT1-A_INTM, respectively. Alternatively, a number of source data streams (e.g., 4) may be interleaved, encoded, and serialized into a single serial stream. Each of the serial streams generally has a signaling rate that is the source data stream data rate multiplied by the number of source streams interleaved (e.g., 2) and the parallel-to-serial conversion ratio (e.g., 10).

The circuit 142 may comprise a circuit 156 and a circuit 158. The circuit 156 may be implemented as a deserializer and decoder circuit. The circuit 158 may be implemented as a bonding and de-interleaving circuit. The circuit 156 may have a number of inputs 160a-160m that may receive the signals B_SER1-B_SERM and a number of outputs 162a-162m that may present a number of signals (e.g., B_INT1-B_INTM) to a number of inputs 164a-164m of the circuit 158. The signals B_INT1-B_INTM may comprise deserialized and decoded interleaved character (data) streams recovered from the serial streams B_SER1-B_SERM. The signals B_INT1-B_INTM may be

skewed from one another due to variance in delays in the respective serial channels.

The circuit 158 may be configured to deskew the signals B_INT1-B_INTM by bonding (aligning) the signals B_INT1-B_INTM to a clock extracted (recovered) from one of the received data streams (e.g., a recovered clock) or to common reference clock. When the signals B_INT1-B_INTM are deskewed, the circuit 158 may be configured to recover (de-interleave) the source data streams (e.g., B_SRC1-B_SRCN) contained within the signals B_INT1-B_INTM. The circuit 158 may have a number of outputs 166a-166n that may present the signals (source data streams) B_SRC1-B_SRCN.

Referring to FIG. 4, a detailed block diagram of the circuit 158 is shown. The circuit 158 may be implemented as a bonding and de-interleaving circuit. The circuit 158 may comprise a circuit 170 and a circuit 172. The circuit 170 may be implemented as a bonding circuit. The circuit 172 may be implemented as a de-interleaver circuit. The signals B_INT1-B_INTM may be presented to inputs of the circuit 170. The circuit 170 may be configured to generate a number of signals B_BND1-B_BNDM in response to the signals B_INT1-B_INTM. The signals B_BND1-B_BNDM may represent bonded (aligned) character streams recovered from the

signals B_INT1-B_INTM. The circuit 170 may have a number of outputs that may present the signals B_BND1-B_BNDM to a number of inputs of the circuit 172. The circuit 172 may be configured to de-interleave the bonded interleaved character streams B_BND1-B_BNDM to recover the source data streams B_SRC1-B_SRCN. The circuit 172 may have a number of outputs that may present the source data streams B_SRC1-B_SRCN.

Referring to FIG. 5, a block diagram illustrating an example operation of the present invention is shown. In one example, the circuit 100 may be configured to communicate four source character streams operating at a rate of 77.75 MB/s (e.g., the blocks 202a-202d). The circuit 100 may interleave (multiplex) the four source character streams, in one example, into two interleaved character streams (e.g., the blocks 204a and 204b). The interleaved character streams may be encoded and serialized (e.g., the blocks 206a and 206b) and transmitted via serial channels (e.g., fiber, coax, twisted pair, etc.) at a rate of 1555MBd (e.g., the links 207a and 207b). The serial streams may be received, deserialized, and decoded back to interleaved character streams (e.g., the blocks 208a and 208b). However, the serial streams may be skewed due to different delays in the links 207a and

207b. The interleaved character streams may be bonded to a common time reference (e.g., the blocks 210a and 210b). When the interleaved character streams are bonded to the common time reference, the interleaved character streams may be de-interleaved (de-multiplexed) to recover the original source character streams (e.g., the blocks 212a-212d).

Referring to FIG. 6, a block diagram of a circuit 100' illustrating an alternate embodiment of the present invention is shown. In an alternative example, a 4:1 interleaving ratio may allow a single serial channel to communicate all of the source streams. Four-to-one interleavers 112' and 114' may be implemented to reduce the number of serial channels to one channel in each direction. Reducing the number of serial channels may reduce the cost of a communication system. However, when higher interleave ratios are implemented, the signaling rate of the serial interface may limit the length of an interconnect (e.g., a copper interconnect).

While the invention has been particularly shown and described with reference to the preferred embodiments thereof, it will be understood by those skilled in the art that various changes

in form and details may be made without departing from the spirit and scope of the invention.